CLAIMS

1. A computing device on a monolithic integrated circuit for multiplying together a digitized multiplier signal value and a digitized multiplicant signal value, said computing device comprising:

an input interface that receives said multiplicant and provides a received multiplicant indicative thereof;

a first place shifting device that includes a first logical assignment circuit to shift data bits of said received multiplicant in response to a first shift command signal, and provides a first shifted signal indicative thereof;

a second place shifting device that includes a second logical assignment circuit to shift data bits of said received multiplicant in response to a second shift command signal, and provides a second shifted signal indicative thereof;

means for summing said first and second shifted signals to provide a summed signal value that is indicative of the product of said multiplier and said multiplicant; and

a control device that receives a signal indicative of said multiplier, and generates said first and second shift command signals indicative of said multiplier value.

2. The computing device of claim 1, comprising a memory device for storing said summed signal, and for providing past values of said summed signal value.

3. The computing device of claim 2, wherein said means for summing receives and sums a

signal value from said memory device indicative of a past value of said summed signal value with said first and second shifted signals to provide said summed signal value.

4. The computing device of claim 1, wherein said first place shifting device comprises a first sign inverter that receives and inverts the sign of said received multiplicant to provide a sign inverted received multiplicant signal that is input to said first logical assignment circuit for bit shifting.

5. The computing device of claim 4, wherein said second place shifting device comprises a second sign inverter that receives and selectively inverts the sign of said received multiplicant to provide a second sign inverted received multiplicant signal that is input to said second logical assignment circuit for bit shifting.

6. The computing device of claim 1, wherein said control unit generates a first sign inversion command signal in response to said multiplier value, wherein said first sign inversion signal is input to said first sign inverter to selectively enable the sign inversion.

7. A computing device on a monolithic integrated circuit for multiplying together a digitized multiplier signal value and a digitized multiplicant signal value, said computing device comprising:

an input interface that receives said multiplicant and provides a received multiplicant indicative thereof;

first means for shifting data bits of said received multiplicant in response to a first shift command signal, and for providing a first shifted signal indicative thereof;

second means for shifting data bits of said received multiplicant in response to a second shift command signal, and for providing a second shifted signal indicative thereof;

means for summing said first and second shifted signals to provide a summed signal value that is indicative of the product of said multiplier and said multiplicant; and

a control device that receives a signal indicative of said multiplier that is a binary coded number using canonical form, and generates said first and second shift command signals indicative of said multiplier value.

8. The computing device of claim 7, comprising a memory device for storing said summed signal, and for providing past values of said summed signal value.

9. The computing device of claim 8, wherein said means for summing receives and sums a signal value from said memory device indicative of a past value of said summed signal value with said first and second shifted signals to provide said summed signal value.

10. The computing device of claim 7, wherein said first means for shifting comprises a first sign inverter that receives and inverts the sign of said received multiplicant to provide a sign inverted received multiplicant signal that is input to said first logical assignment circuit for bit shifting.

11. The computing device of claim 10, wherein said second means for shifting comprises a second sign inverter that receives and selectively inverts the sign of said received multiplicant to provide a second sign inverted received multiplicant signal that is input to said second logical assignment circuit for bit shifting.

12. A computer unit for a first (z) and a second (k, k*) number comprising:

at least one place shifting device (3, 4), whose shift position is controlled by an associated shift instruction (s1, s2) in dependence on the second number (k, k*), and to whose position inputs are conducted the value-ordered places of the first number (z), which generally is a binary coded dual number;

the input or output of each place shifting device (s1, s2) has associated with it a sign inverter (5, 6), which is controlled by an associated sign instruction (n1, n2), in dependence on the second number (k, k*), which generally is a binary coded dual number using the canonical form;

on the output side, each place of the place shifting device (3, 4) is connected respectively to a place input of a four-place adder (7); and

the functions such as place shifting, negation, and addition run as completed function executions within a single clock cycle or time-staggered in a pipeline process extending over at least two clock cycles.

13. The computing unit of claim 12, wherein the number of place shifting devices (3, 4) that can be controlled independently of one another depends on the choice of the second number (k, k*), mainly on the maximum number of places of the second number (k, k*), which is determined

by this choice, the places with the value zero being excluded from the considered set of places.

14. The computing unit of claim 12, wherein in the shift instruction (s1, s2) for the particular place shifting device (3, 4), a shift position is also defined for which the outputs for the following adder (7) are blocked or are set to zero.

15. The computer unit of claim 14, wherein the output places of the adder (7) are coupled to the inputs of a summation memory (8).

16. The computer unit of claim 15, wherein a summation instruction (ak) activates a data path that correctly feeds back the place outputs of the summation memory (8) to the adding inputs of the adder (7).

17. The computer unit of claim 16, wherein the first number (z) and the second number (k, k*) are binary coded dual numbers, and that the first and second number (z and k, k*), are multiplied by successive shift processes of a single place shifting device (3), the particular shift positions being determined by successive shift instructions (s1), in dependence on the values of the associated binary places of the second number (k, k*).

18. The computer unit of claim 17, wherein if two or more place shifting devices (3, 4) are present, the successive shift processes take place by groups, in that a binary position of the second

number (k, k*) is associated with each place shifting device (3, 4), the associated binary positions of the second number being determined by successive shift instructions (s1, s2).